TECHNICAL PROGRAM
LASCAS / IBERCHIP / LAEDC

8 am **Opening Ceremony**
Monday, February 25, Uruma Room

8:30 am **Keynote: New trends in electronic systems: Technology, circuits and architecture**

Giovanni De Michelli
Institute of Electrical Engineering and of the Integrated Systems Centre at EPF Lausanne, Switzerland

This talk will address the needs of new emerging technologies, such as 2-dimensional nanoelectronics, optical devices and quantum devices in terms of design support through computer aids. I will present the circuit abstractions, as well and design methods to achieve competitive circuits. I will show where existing tools and flows can be used and where new algorithms and data structures are needed in the search of the best match between devices and architectures. I will conclude with some examples of emerging designs.

9:30 am **BREAK**

10 am **Keynote: Will Democratic Artificial Intelligence Shape the Future of Semiconductor Technology?**

Adrian M. Ionescu
Nanolab, Ecole Polytechnique Fédérale de Lausanne, Switzerland

In this talk we will discuss the present and future challenges of semiconductor devices and technologies in terms of scaling and energy efficiency, with main focus on Edge Artifical Intelligence applications. We will illustrate the talk with examples of near-100mV electronic steep slope devices and sensors. We will particularly show the there is a need to anticipate and address future Digital Hardware challenges with focus on the Edge Computation and technology-system-algorithm related topics such as: machine learning on the Edge, energy efficiency, custom form factors, close to real-time operation, enhanced security features and enhanced customer experiences.

11 am PARALLEL SESSIONS

Monday, February 25

Session 1-1A: LASCAS - Biomedical Circuits and Systems
Monday, February 25, 11:00 am, Pamba 1 Room
Session Chair: I. Jaramillo

C31 **Low Noise Front-End and ADC for Real-Time ECG System in CMOS Process**
11:00 am Pablo Gardella, Emanuel Villa Fernandez, Eduardo Baez, Nicolás Biberidis and Juan Cesaretti

This paper presents the design and experimental results of a digital acquisition system based on a chopper-stabilized Instrumentation Amplifier with Common-Mode feedback for CMRR enhancement. Chopping techniques are used to remove both offset and flicker noise, detrimental effects characteristic of pure CMOS processes. A second-order, discrete-time, single-bit Sigma-Delta ADC with CIFB structure is used to convert the signal into the digital domain where it can be processed in real time to diagnose and report urgencies. Measurements on a 0.6µm process have shown that the input CMRR is boosted by 71dB when the feedback is closed through the patient. The input referred integrated noise for the overall system within the ECG band frequencies of 0.1Hz to 400Hz (including the quantization noise) is 4.2µVP, below the recommended maximum detection error of 10.0µVP.

C70 **Prototyping a Biologically Plausible Neuron Model on a Heterogeneous CPU-**
11:20 am **FPGA Board**
Kaleb Alfaro-Badilla, Carlos Salazar-García, Alfonso Chacon-Rodriguez, Georgios Smaragdos, Christos Strydis, Andrés Arroyo-Romero and Javier Espinoza-González

A heterogeneous hardware-software system implemented on an Avnet ZedBoard Zynq SoC platform, is proposed for the computation of an extended Hodgkin Huxley (eHH), biologically plausible neural model. SoC's ARM A9 is in charge of handling execution of a single neuron as defined in the eHH model, each with a O(N) computational complexity, while the computation of the gap-junctions interactions for each cell is offloaded on the SoC's FPGA, cutting its O(N^2) complexity by exploiting parallel-computing hardware techniques. The proposed hw-sw solution allows for speed-ups of about 18 times vis-à-vis a vectorized software implementation on the SoC's cores, and is comparable to the speed of the same model optimized for a 64-bit Intel Quad Core i7, at 3.9GHz.

Session 1-1B: LASCAS - DSP
Monday, February 25, 11:40 am, Pamba 1 Room
Session Chair: L. Agostini

C33 **Recognition of emotions using ICEEMD-based characterization of multimodal**
11:40 am **physiological signals.**
Andrés Ordóñez Bolaños, Jeferson Gomez Lara, Diego Hernan Peluffo Ordóñez, Daniela Medrano David, Carolina Duque Mejia, Cristian Mejia Arboleda and Miguel Alberto Becerra Botero

The emotions identification is a very complex task due to depending on multiple variables individually and as a group. They are evaluated by different criteria such as arousal, valence, and dominance mainly. Multiple researches have been focus on building prediction systems, nevertheless, this is still anopen research field. The main objective of this paper is the analysis of the improved complete empirical mode decomposition (ICEEMD) for feature extraction from physiologicalsignalsforemotionsprediction.Physiologicalsignalsandmetadata of the DEAP database were applied. First, the signals were preprocessed, then three decompositions were carried out using ICEEMD, discrete wavelet transform (DWT), and Maximal overlap DWT. Feature extraction was carried out using Hermite coefficients, and multiple statistic measures from IMFs, coefficientsDWTandMODWT,andsignals.Then,ReliefFselectionalgorithmswere applied for reducing the dimensionality of the feature space. Finally, LDC and K-NN cascade

classifiers were tested. The different decomposition techniques were compared and relevant signals and measures were established. The results demonstrated the capability of ICEEMD decomposition for emotions analysis from physiological signals.

C52 12:00 pm **ASC-FFT: Area-efficient low-latency FFT design based on asynchronous stochastic computing**

Patricia Gonzalez-Guerrero, Xinfei Guo and Mircea Stan

Asynchronous Stochastic Computing (ASC) is a new paradigm that addresses synchronous Stochastic Computing (SSC) drawbacks, expensive stochastic number generation (SNG) and long latency, by using continuous time streams (CTS). To go beyond the basic operations of addition and multiplication in ASC we need to incorporate a memory element. Although for SSC the natural memory element is a clocked-flip-flop, using the same approach with no synchronized data leads to unacceptable large error. In this paper, we propose to use a capacitor embedded in a feedback loop as the ASC memory element. Based on this idea, we design a low-error asynchronous adder that stores the carry information in the capacitor. Our adder enables the implementation of more complex computation logic. As an example, we implement an asynchronous stochastic Fast Fourier Transform (ASC-FFT) using a FinFET1X1 technology. The proposed adder requires 76%-24% less hardware cost compared against conventional and SSC adders respectively. Besides, the ASC-FFT shows 3X less latency when compared with SSC-FFT approaches and significant improvements in latency and area over conventional FFT architectures with no degradation of the computation accuracy measured by the FFT Signal to Noise Ratio (SNR).

Session 1-2: LASCAS - Analog Circuits and Systems

Monday, February 25, 11:00 am, Uruma Room
Session Chair: A. Arnaud

C97 11:00 am **An All-Thin-Devices Level Shifter in Standard-Cell Format for Auto Place-and-Route Flow**

Nestor Cuevas, Javier Ardila and Elkim Roa

This paper proposes a standard-cell format all-thin-devices level shifter suited for commercial digital-flow tools. Despite the fact that it is possible to find commercial level-shifter cells in standard-cell format, those cells require a mixed of thick- and thin-devices. The use of only thin-oxide transistors allows placing level shifters within thin-device based digital cells, optimizing area and place-and-route process. Due to the maximum voltage ratings of thin transistors, we adopted a switching technique to prevent high voltage differences between their terminals, avoiding a possible device breakdown. The proposed level shifter occupies an area of 156um^2 in a 0.18um CMOS node.

C84 11:20 am **Performance evaluation of Tunnel-FET basic amplifier circuits**

Roberto Silva, Paula Agopian and João Martino

This work analyzes the performance of measured Tunneling Field-Effect Transistors (TFET) when applied to analog circuits. The method uses a look-up table based behavioral model, taking the experimental results from a fabricated silicon pTFET as input. The Verilog-A behavioral language is used to implement the TFET model, enabling the use with spice-like simulators along with passive and active elements, achieving bigger circuits than other implementations involving numerical multiphysics simulation of the device. The model is further incremented with device capacitances, and the response of analog circuits is considered. An Operational Transconductance Amplifier (OTA) is presented, showing near 130 dB open-loop gain and 18.9nW power consumption.

C82 11:40 am **Evaluation of Distortion Level in Analog Multipliers through DC Analysis Only**

Gabriele Goncalves, Mário Silva, Fabian Andrade, Fernando Cardoso, Antônio Sousa, Edson Santana and Ana Isabela Cunha

This work presents a methodology for determining figures of merit to assess distortion in analog multipliers using only DC analysis. Besides the direct determination of two dimensional integral

nonlinear function, the distortion coefficients are calculated to fit the DC transfer surface and are used to estimate the total harmonic distortions for single and double input. Simulation and experimental results demonstrate that figures of merit determined either by AC or DC analysis agree with enough reliability.

C21 **Voltage CMOS Quaternary Gates for Digital Designs**
12:00 pm Milton Ernesto Romero Romero, Evandro Mazina Martins, Danillo Christi, Alexandro De Moraes Nogueira and Mario Enrique Duarte González

To take advantage of the Multiple Valued Logic, with domain: {0, 1, . . . , N − 1}, where N is the base of representation, a set of integrated circuits (IC) that implement the MVL operators is needed. In the IC implementation, it is necessary to minimize the number of transistors to improve area utilization and power consumption, among other advantages. This work proposes an implementation of gates: Successor, eAND1, eAND2, eAND3, and MAX, with only 25, 14, 28, 6 and 3 MOS transistors, using Austriamicrostystems 0.35µm technology; such that, the number of utilized transistors in the proposed implementation is lower than the number of transistors for equivalent gates reported in literature.

Session 1-3: LAEDC - Devices and materials
Monday, February 25, 11:00 am, Pamba 2 Room
Session Chair:

E9 **Effect of Drain Top Metal Overlap on the Current in Bottom-gate Thin Film**
11:00 am **Transistors**
Magali Estrada, Isai Hernandez, Yoanlys Hernandez-Barrios, Matteo Rapisarda, Antonio Valletta, Luigi Marucci and Antonio Cerdeira

In this paper we analyze the effect of the top metal overlap associated to the drain contact, that can be present in thin film transistors (TFTs) with bottom-gate staggered configuration. It is shown that the effect of the top metal contact at the drain, overlapping the passivation or etch stopper layer (ESL), increases the drain current. Results from numerical simulations show that this top metal overlap acts as a second gate to the device, partially located near the drain contact. The overall effect on the device current will depend on the semiconductor doping, as well as on the thickness and dielectric constants of the gate dielectric and passivation/ESL layers. The effect is more significant as the channel length of the devices is reduced.

E11 **Comparison of Different Technologies for Transistor Rectifiers Circuits for**
11:20 am **Micropower Energy Harvesters**
Luis-Miguel Procel-Moya, John Paredes and Lionel Trojman

The present work shows the comparison of planar CMOS, FinFET and Tunnel-FET technologies in the principal full-wave rectifier circuits. Rectifier circuits are fundamental part of energy harvester systems. We have chosen the conventional, the gate cross-coupled and the fully cross-coupled rectifiers topologies for circuit simulation. Simulations are carried on Custom-Compiler and HSPICE platform from Synopsys. We measure the average value factor, the ripple voltage and the ripple factor. We obtain that FinFET and Tunnel-FET technologies are the best candidates to work in low voltage. As well, we analyze that the fully cross-coupled topology is the one that best behaves as pure rectifier. In addition, we show that all technologies behave as a combination of rectifier and filter in high frequency

E3 **Substrate influence on Bi2Te3 growth by MBE.**
11:40 am Omar Concepción Díaz, Osvaldo de Melo and Arturo Escobosa

Bi2Te3 epitaxial films were obtained on Al2O3 and SrTiO3 by molecular beam epitaxy. Morphological and structural studies on the films deposited on both substrates showed no significant differences. ARPES measurements displayed similar Dirac cones in both samples. We propose that van der Waals interactions compensate the lattice mismatch between Bi2Te3 and Al2O3 and SrTiO3 allowing epitaxial growth.

E12 12:00 pm **High Efficient Inverted Polymer Solar Cells with Solution-Processed Electron Transport Layer.**
José G. Sánchez, Víctor S. Balderrama, Magali Estrada, Josep Pallarès and Lluis F. Marsal

We demonstrate highly efficiency inverted polymer solar cell (iPSCs) based on PTB7:PC70BM and PTB7-Th:PC70BM. The effects of solution-processed TiOx, ZnO and PFN as electron transporting layer (ETL) on the performance of iPSCs are investigated. Devices using ZnO as ETL exhibit the highest power conversion efficiency (PCE = 9.5%). Additional impedance spectroscopy measurements demonstrate that charge carrier collection in iPSCs is limited by the series and shunt resistances driven by the hole transporting layer.

Session 2: INDUSTRY PANEL
Monday, February 25, 2:00 pm, Uruma Room

4 pm **BREAK / DEMO SESSION**

4:30 pm **PARALLEL SESSIONS**
Monday, February 25

Session 3-1: Special Session "High-Speed Circuit Design and Analysis"
Monday, February 25, 4:30 pm, Pamba 1 Room

SS1 4:30 pm **Composite Resistor Technique for Process and Temperature Compensations of Low Power Ring Oscillators**
Hakan Cetinkaya, Ali Zeki, Alper Girgin and Tufan Coskun Karalar

A process and temperature compensation technique, namely, composite resistor, is adopted for the current controlled oscillators (CCOs). The core is a ring oscillator (RO) and oscillates at 1 MHz at room temperature (25oC) with 50% duty cycle. The temperature compensation is achieved between -20oC and 100oC, and after trimming, the inaccuracies of the output frequencies, 1 MHz, and 0.5 MHz, are below ±1% (3σ) in the same temperature range. As a result, 2 outputs are temperature compensated. The oscillator core consumes 750 nA, the biasing circuit consumes 360 nA, and the complete system consumes 1.256 µA, corresponding to 2 µW at 1.6 V battery voltage. The design, occupying 130 µm × 285 µm die area, is realized in a 0.18 µm Mixed-Signal RF Salicide (1P6M, 1.8V/3.3V) CMOS process.

SS2 4:50 pm **A Segmentation Algorithm for Capacitively Loaded Planar Resonant Structures**
Ihsan Erdin and Ram Achar

The segmentation method used for the analysis of arbitrarily shaped planar structures is extended to a more general form to account for capacitive loading between parallel plates. In power integrity (PI) analysis of power delivery networks (PDN), the capacitive loading represents decoupling capacitors between power and ground planes. The algorithm is geared to the analysis of PDNs for performance evaluation, selection and placement of decoupling capacitors. For linear circuits, the proposed integrated algorithm eliminates the commonly used two-step approach. In the case of nonlinear loads, the algorithm helps to reduce the size of modified admittance matrix (MNA) and relaxes the burden of following circuit simulation. The proposed method is validated in comparison to a numerical electromagnetic (EM) simulator. Index Terms—power delivery network, decoupling capacitors, power integrity, optimization, segmentation method.

SS3 5:10 pm **LIM Algorithms for MOSFET Models**
Jose Schutt-Ainé and Patrick Goh

This paper introduces algorithms for the simulation of MOSFETS using the latency insertion method (LIM). The algorithms are independent of the MOSFET model level chosen and account for current and charge effects. The latency insertion method (LIM) has been demonstrated as an optimum algorithm for the transient simulation of large networks. In particular, we address the generation of the update equations. Examples and comparisons are given for evaluating the algorithms.

SS4 5:30 pm **Behavioral Modeling of Pre-emphasis Drivers Including Power Supply Noise Using Neural Networks**
Huan Yu, Mourad Larbi and Madhavan Swaminathan

This paper addresses the nonlinear behavioral modeling of pre-emphasis drivers including power supply noise. The proposed multiple-port model relies on the use of power-aware weighting functions that control the driver's output stage to model the pre-emphasis behavior with non-ideal power supply accurately. The weighting functions are implemented using feed-forward neural networks (FFNNs), and the dynamic memory characteristics of driver's ports are captured using recurrent neural networks (RNNs). Practical industrial driver example demonstrates that the proposed modeling method offers good accuracy, flexibility and significant simulation speed-up to facilitate signal integrity and power integrity analysis without compromising intellectual property (IP).

Session 3-2: LASCAS - Analog Circuits and Systems
Monday, February 25, 4:30 pm, Pamba 2 Room
Session Chair: E. Roa

C87 4:30 pm **CNN Learning for Image Processing: Center of Mass versus Genetic Algorithms**
Fabian de Andrade, Ana Isabela Cunha, Edson Santana, Eduardo Simas Filho, Gabriele Gonçalves and Antonio de Sousa

This paper presents a comparative performance analysis of two learning algorithms developed for the use in Cellular Neural Networks (CNN): the Center of Mass Algorithm, a back-propagation like technique, and an adaptation of the Genetic Algorithm. Both methods are applied for training of a CNN built with Full Signal Range (FSR) cells, for the implementation of several well-known bipolar functions of image processing. Performance parameters such as total execution time, number of CNN runs and success rates are assessed in order to provide guidelines for the learning method choice.

C110 4:50 pm **An asymmetrical bulk-modified composite MOS transistor with enhanced linearity**
Alfredo Arnaud, Rafael Puyol, Alfonso Chacón, Matias Miguez and Joel Gak

In this work, an asymmetrical bulk-linearized composite MOSFET is presented, with an enhanced linear range and an equivalent saturation voltage of up to several hundred mV even in weak inversion, allowing to implement large MOS resistors. Some preliminary measurements are presented, as well as 150MΩ and 200MΩ equivalent resistors simulations, with up to 1.5V linear range. A low frequency, 40dB gain, fully integrated cardiac sensing channel filter/amplifier is also shown, taking advantage of the proposed technique to consume only 25nA supply current.

C107 5:10 pm **A 1.8V 9bit 10MS/s SAR ADC in 0.18 µ m CMOS for bio-impedance analysis**
Daniele Dos Santos, Hugo Hernandez and Wilhelmus Van Noije

This paper presents a power-efficient 9bit 10MS/s SAR asynchronous ADC for bioimpedance analysis. The prototype was designed using 180nm TSMC CMOS technology. The ADC core occupies an active area of 0.124mm². The ADC main parameters were extracted from layout for simulations, which resulted in an SNR of 55.29dB and an ENOB of 8.59 bit at 1.8V supply while consuming 0.692mW, resulting in a Figure of Merit (FoM) of 145.93 fJ/conversion-step.

C8 **A 13-nW Voltage Reference with Orthogonal Trimming of Absolute Value and**
5:30 pm **Temperature Coefficient**
Jader A De Lima and Fortunato C. Dualibe

An all-MOSFET voltage reference generator (VRG) with a trimming approach that permits orthogonal fine-tuning of VREF and temperature coefficient (TC) has been designed in 0.18 □m CMOS process. SPICE simulations back up theoretical analysis. With devices operating in deep-subthreshold, the VRG complies with VDD as low as 0.5V, yielding nominal VREF=239.9mV and TC =14.6ppm/oC. Considering all process corners, for 0.5V ≤ VDD ≤ 1.5V and -40oC ≤ T ≤ 120oC, post-trimming yields maximum spread of 1.63% and 34.5ppm/oC, respectively for □VREF/VREF and TC. Typically, consumption is only 13nW@120oC, accounting for trimming and startup circuits. Line regulation of 0.21%/V and rejection to supply-line noise of 115.5dB@100MHz are also foreseen. Monte Carlo reveals post-trim 0.9% (3σ) accurate VREF.

Session 3-3: LAEDC - Modeling
Monday, February 25, 4:30 pm, Pamba 3 Room
Session Chair:

E1 **UMEM based 1/f noise model for amorphous ESL IGZO TFTs**
4:30 pm Wondwosen Eshetu Muhea, Thomas Gneiting and Benjamin Iñiguez

this work presents a physics-based model for the flicker (1/f) noise behavior of bottom-gated amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) with an Edge-Stop Layer (ESL). The model is derived based on the so-called Unified Method and Extraction Procedure (UMEM), a technique previously used in accurate device parameter extraction and simulation of current-voltage (I-V) characteristics of the amorphous hydrogenated Silicon (a-Si:H), polycrystalline Silicon (poly-Si), and Organic TFT (OTFT) devices. It has been reported that 1/f noise in the bottom-gated a-IGZO TFT with ESL and with a very thin film IGZO layer obeys the carrier number fluctuation theory. The unified 1/f noise model is, therefore, adapted here to take into account the correlated bulk mobility fluctuation as well. Excellent agreements of the model with measured DC and flicker noise characteristics have shown the model validation

E5 **Full SPICE Simulation of a CMOS Active Pixel Sensor with Generalized Devices**
4:50 pm Chiara Rossi and Jean-Michel Sallese

We present SPICE simulations of a CMOS APS pixel element consisting of the optical sensor and the circuit. The photodiode is simulated at the physics level by means of the socalled generalized devices, without any predefined compact model. Conversely, regular compact models are used for MOSFETs. Modeling with Generalized Devices takes into account in SPICE simulations both the layout and the physics of the photodiode, that is drift-diffusion transport, optical generation and recombination of excess carriers, capacitive effects and surface recombination. This approach is supported by TCAD simulations and opens the way to full SPICE simulation of Active Pixel Sensor down to the semiconductor level.

E6 **Parameter extraction and modeling of OTFTS from 150K to 300K.**
5:10 pm Harold Cortes-Ordonez, Clara Haddad, Stephanie Jacob, Gerad Ghibaudo, Firas Mohamed, Magali Estrada, Antonio Cerdeira and Benjamin Iniguez

We target the parameter extraction and modeling of organic thin film transistor (OTFTs) from 150K up to 300K. We also analyze the temperature dependence of the extracted parameters. For that propose, we used the unified model and parameter extraction method (UMEM). We validated our adjusted model by comparison with experimental I-V characteristics in both the linear and saturation regimes.

E7 **Charge-Based Compact Modeling of Capacitances in Staggered OTFTs**
5:30 pm Jakob Leise, Jakob Pruefer, Ghader Darbandy and Alexander Kloes

This paper introduces a charge-based approach to model the total charges and the capacitances in staggered organic thin-film transistors (OTFTs). The charges are calculated by integrating over the charge density per gate area along the whole channel. The charges associated with the drain and source terminals are yielded by applying a linear charge partitioning scheme. A series of substitutions is done so that finally the total charges can be calculated in dependence on the charge densities at the drain/source end of the channel. The equations are implemented in an already existing DC compact model. For verification purposes TCAD simulation data and measurements are used. The compact model shows a good agreement with TCAD data and also agrees with measurement data to a certain degree. The advantage of the model is that it has one unique formulation that covers all operation regimes and it is physicsbased.

8:30 am **Keynote: The INTERNET of everything: What´s missing?**
Tuesday, February 26, Uruma Room

Thomas Lee
Stanford School of Engineering, Stanford University, USA

Wireless technology has evolved through three distinct ages. A fourth age -- the Internet of Everything -- is poised to explode and take us to terascale connectivity. But one trillion is a huge, almost incomprehensible number. It is so huge, in fact, that scaling presents both a qualitative and quantitative challenge. Are there enough engineers to design all of these devices? Will the economics of making chips have to change fundamentally? How are we going to provide power for all of these things? Do we need new protocols and standards? How about circuits? This talk will consider impediments to achieving the terascale and what engineers should be thinking about now to make sure that we can get to the terascale sooner than later.

9:30 am **BREAK**

2 pm **PARALLEL SESSIONS**
Tuesday, February 26

Session 4-1: LASCAS - Digital Circuits and Systems
Tuesday, February 26, 2:00 pm, Uruma Room
Session Chair: A. Chacon

C11 **Memristor device fabricated from doped graphene oxide**
2:00 pm Marina Sparvoli, Mario Gazziro, Jonas Marma and Gabriel Zucchi

Resistive switching (RS) is the basic phenomenon for the operation of resistive memory ReRAM. A specific electrical voltage is applied in the MIM (metal-insulator-metal) device, it can undergo switching from its initial insulator resistance state (HRS - high resistance state) to a low resistance state (LRS). There is a strong relationship between the materials used in the composition of these devices and their characteristics. In this work, resistive memory based on silver-doped graphene oxide was characterized and its voltage response varying as a function of voltage was obtained. SET and RESET are caused by the redox reactions of graphene oxide layer at the interface between electrodes. Defects as oxygen vacancies in oxide material play a key role for the resistive switching. There is another factor that can influence the operation of this device and threshold switching: silver present in the graphene oxide composition could interfere with the filament formation. In summary, the resistive switching behavior of a rGO+0.1%Ag/GO+1%Ag/Al device was investigated, which reveals electric characteristics and SET/RESET voltages. In addition, a threshold switching characteristic is revealed.

C28 **Introducing Asymmetry in a CMOS Latch to Obtain Inherent Power-On-Reset**
2:20 pm **Behavior**
Fabian L. Cabrera, Fernando Rangel de Sousa and Hector Pettenghi

A very important characteristic of sequential circuits is the initial state of the registers. Commonly, it is not possible to guarantee the logic value of the registers after the energizing of the circuit, so their initial values are forced through a Power-On-Reset module. In this paper we propose an asymmetric alternative to the conventional CMOS latch topology, which ensures its initial stored value without the use of additional circuits. We present the theoretical considerations that determine the initial state in the conventional and new topologies. Since the geometry of the transistors used to create the asymmetry is equal to that of the conventional circuit, the same occupied area is kept. A flip-flop was fabricated in CMOS 130nm using both topologies. The measurements over 16 different samples demonstrated the correct functionality of the new topology when compared to the conventional one.

C45 **Power-Efficient Approximate SAD Architecture with LOA Imprecise Adders**
2:40 pm Roger Porto, Luciano Agostini, Bruno Zatt, Nuno Roma and Marcelo Porto

Approximate computing is a highly promising approach to reduce the computational effort in video encoders. Its use is even more relevant and advantageous when high resolution videos must be processed in real time using battery powered devices. In this scenario, it is essential to reduce power dissipation and silicon area. In particular, the distortion metric calculation module is one of the most time demanding and the Sum of Absolute Differences (SAD) is usually the most used distortion metric, mainly when dedicated hardware is considered. To overcome this demand, this paper presents a power-efficient SAD architecture compliant with current video encoders based on the usage of Lower-Part-OR Adders (LOA). The attained results showed that important power (17.99%) and area (30.56%) savings can be reached, with an increase of only 0.3% in BD-rate. When compared with state of the art related works, the designed architecture reaches the best area and power dissipation results.

C65 **Process Variability Challenges for Radiation Mitigation Techniques on 16nm**
3:00 pm Samuel Toledo, Ricardo Reis and Cristina Meinhardt

This paper investigates the impact of process variability on traditional radiation and noise mitigation techniques on deep nanometer bulk CMOS technology. Schmitt Trigger, Strengthening, Pseudo-Strengthening, and Rad-Hard techniques are explored observing the sensitivity to process variability. Results shows that these techniques operating under process variability can introduce large degradation on timing and power. This study presents the benefits, and the drawbacks brought from the applied techniques.

Session 4-2: LASCAS - Electronic Testing and Fault Tolerant Circuits
Tuesday, February 26, 2:00 pm, Pamba 1 Room
Session Chair: E. Sanchez

C93 **Post-Silicon Debugging Platform with Bus Monitoring Capability to Perform**
2:00 pm **Behavioral and Performance Analyses**
Wilmer Ramirez and Elkim Roa

Post-silicon debugging systems must offer run-control capability and visibility on complex SoC in order to detect/analyze errors and find possible design enhancements. This paper presents a scalable and reusable debugging platform for post-silicon validation. The platform is composed of a debug module with JTAG communication and a bus monitor. Relevant features are core control, system bus operation, and non-intrusive monitoring. A flexible filtering allows selecting transfers of interest or performing a general monitoring of the SoC. Captured data can be analyzed by performance counters that check executed and finished transfers, calculating their latency to detect deadlocks in the system. The debugging platform has been implemented as part of a SoC with a 32-bit RISC-V based core and multiple peripherals.

C73 **Facilitating Fault-Simulation Comprehension Trough a Fault-Lists Analysis Tool**
2:20 pm Davide Piumatti, Paolo Bernardi and Ernesto Sanchez

The complexity of modern embedded processors used in safety-critical applications requires in-field self-test strategies. The most popular ones are based on hardware and software-based approaches such as Logic-BIST (L-BIST) and Software-Based Self-Test (SBST). While the first one requires to include in the device additional hardware, the second one consists on the execution of a set of assembly programs, usually called a Software Test Library (STL). In this context, if the SLT strategy is adopted for in-field testing of the device, a very time consuming task is necessary to validate the final results of the test library. This process, that includes the fault simulation of every test program, should determine the actual contribution that a given test may provide to the final test library, by computing intermediate results manipulating, comparing, including, and excluding the test program results with respect to all the others. This task is useful, for example, to understand whether the changes made to a test program produced a gain in the final fault coverage or not. In this paper, we propose for the very first time, a Fault List Analysis Tool that is able to support the development of a STL by performing some fault-list oriented operations on the preliminary results obtained during the development process. The analyzes provided by this new tool are not implemented in commercial tools. Some experimental results were gathered during the STL development for various processors developed by STMicroelectronics.

C4 2:40 pm **A Low Noise Fault Tolerant Radiation Hardened 2.56 Gbps Clock-Data Recovery Circuit with High Speed Feed Forward Correction in 65 nm CMOS**

Jeffrey Prinzie, Szymon Kulis, Pedro Leitao, Rui Francisco, Paulo Moreira and Paul Leroux

A fault tolerant, radiation hardened Clock and Data Recovery (CDR) architecture is presented for high-energy physics and space applications. The CDR employs a novel soft-error tolerant Voltage Controlled Oscillator (VCO) and includes a high-speed feed-forward path to stabilize the CDR to compensate for an additional pole in the VCO to harden it against ionizing particles. The CDR has a data rate of 2.56 Gbps and uses In-Phase/Quadrature (IQ) clocks in combination with a frequency detector (FD) to increase the pull-in range. The circuit was designed in a 65 nm CMOS technology and has a core power consumption of only 34 mW.

Session 4-3: LAEDC - Devices physics

Tuesday, February 26, 2:00 pm, Pamba 2 Room

Session Chair:

E16 2:00 pm **RF and DC degradation of a SOI FET technology**

Edmundo A. Gutierrez-D., Jairo Mendez, Julio Tinoco and Emmanuel Torres-R.

We introduce experimental results of the I-V characteristics degradation of a Silicon SOI technology for RF applications when exposed to both; a 28 GHz and a DC stress input signals. Then we compare the effect of DC and RF stress on threshold voltage and Drain-Induce-Barrier-Lowering reliability. We observe that reliability under RF stress is gate voltage dependent, and in some cases an improvement of the I-V characteristics is observed. A hypothetical explanation for the degradation/enhancement under RF stress is attributed to selfheating and self-healing (SH2).

E4 2:20 pm **Analysis of Vias Position on the BEOL Temperature Distribution**

Rafael Nunes, Jose Bohorquez and Roberto Orio.

A study of the temperature distribution on the BEOL structure and its impact on the electromigration in a design environment has been developed and implemented. The study for a 45 nm technology indicated a large temperature variation from the local to the global interconnects, which should be considered for the EM induced resistance increase of the line, in contrast to the standard analysis through a fixed operation temperature throughout the BEOL. The results show that a significant additional temperature above 30 °C exist on the layers M1 to M11 due the power dissipated from transistors. The temperature reduction on the local layer is evaluated changing position and number of vias, both with a direct influence on the BEOL thermal distribution. The results show a reduction of temperature from 365 K to 358 K for M1 layer, considering a fraction volume of 6 % for vias distributed equally spaced with 2.4 µm.

E2 **IoT Circuit Design to Monitor Cold Chain Refrigerators**
2:40 pm Oscar De Jesús Ballestas Ortega, José Luis Villa Ramírez and Edgar David Villa Pérez

Under the concept of the Internet of Things, was designed a PCB to monitor faults in refrigerators or freezers, which use conventional compressors or non-inverters. It should be emphasized that these equipment belong to a cold chain, where it is considered approximately 2000 refrigerators. This solution includes among its main requirements Sigfox wireless communication, to send data or alarms from refrigerators or end nodes to the server in the cloud. One of the attractions to choose SigFox technology is its low cost as a communication service. Other aspects of design are: control the compressor, alert operational failures, measure the temperature inside the freezer, measure power consumption, voltage and current. Another fundamental requirement of the design is to achieve a low cost in its production to be in the margin of the sale of conventional temperature controllers, perhaps not equal, but not be well above the commercial value. With these premises, the hardware architecture is basically composed by a Switched-Mode Power Supply (SMPS), a control unit with a PIC32, 5V DC relays to switch an output of 220V AC, NTC temperature sensor, Power meter IC, battery charger, Sigfox communication module and EPaper Display.

E17 **Study of the properties of transport in semiconductor devices due to the effect**
3:00 pm **of the static magnetic field.**
Adrian I. Tec Chim, Oscar Huerta and Edmundo Gutierrez

The properties of electronic transport under the influence of hybrid magneto-electric barriers are investigated. Magnetic barriers are of three types: (1) periodic arrangement of delta functions with alternating sign, (2) a single delta function and (3) two delta functions with alternating sign. The results indicate that magneto-electric structures influence energy levels, wave functions and transmission probabilities

Session 4-4: IBERCHIP
Tuesday, February 26, 2:00 pm, Pamba 3 Room
Session Chair:

I1 **Clúster para Computación de Alto Rendimiento basado en plataformas SoC-**
2:00 pm **FPGA**
Juan Hernández, Alejandro Ruiz and Alexander Lopez

Este artículo presenta la construcción de un clúster para Computación de Alto Rendimiento basado en plataformas SoC-FPGA, en este caso se usaron dos nodos cada uno con una tarjeta DE1-SoC, la cual se basa en un dispositivo Cyclone V. El clúster exhibe una arquitectura híbrida que permite hacer uso de los estándares OpenCL, OpenMP y MPI para implementar algoritmos sin requerirse el uso de lenguajes de descripción de hardware para el uso del FPGA. De igual manera, se diseñó una interfaz de usuario que facilita la integración de herramientas y la implementación de algoritmos sobre el clúster. El desempeño del clúster fue evaluado usando un algoritmo de filtrado FIR, el cual fue implementado en software, en hardware y en hardware/software para verificar la aceleración alcanzada por el clúster. Finalmente, los resultados mostraron una aceleración 13 veces superior respecto a la implementación software, también se encontró que el rendimiento del clúster aumenta conforme aumentan el tamaño de la señal de entrada y la complejidad computacional del algoritmo.

I3 **Avaliação de Heurísticas de Trunk Routing Aplicadas ao Roteamento Detalhado**
2:20 pm Eder Monteiro, Mateus Fogaça, Henrique Placido, Jucemar Monteiro, Isadora Oliveira, Marcelo Johann and Ricardo Reis

Este trabalho apresenta uma avaliação de duas heurísticas de trunk routing: o STST (Single Trunk Steiner Tree) e o RST-T (Refined Single Trunk Tree), aplicadas ao roteamento detalhado. Comparamos a eficiência de ambos os algoritmos para gerar a topologia final das nets, considerando o comprimento de fios, número de segmentos e vias, e o número de nets

que cada algoritmo consegue rotear. Resultados experimentais mostram que o RST-T consegue rotear cerca de 5% mais nets do que o STST para os casos de teste sem obstáculos e sem pinos de Power/Ground em camadas de metal superiores e 6% menos nets que o STST quando os benchmarks têm bloqueios nessas camadas. Além disso, o RST-T gera topologias com 1-4% menos comprimento de fio e produz em média 2% menos vias em ambos os casos.

I5 2:40 pm **Design of Locally-Clock Asynchronous State Machines Aimed at FPGAs Based in LUTs**

Duarte de Oliveira, Diego Silva, Gracieth Batista and Leonardo Romano

Controllers based on Synchronous Finite State Machines (SFSM) are widely used in the control unit design of complex digital systems. These systems can be implemented in Field Programmable Gate Arrays (FPGAs) and they can present serious problems related to global clock, such as: clock skew and increased power consumption related to the clock. In this context, the asynchronous paradigm shows interesting features that fit as an alternative for the design. The Asynchronous FSMs implemented in the FPGA platform are strongly subject to essential hazard due to significant delays between logical blocks. A key hazard solution is to insert delay elements into AFSM feedbacks, which in the FPGA platform can be a difficult task. This paper proposes two new architectures and two new methods for synthesis of locally-clock AFSMs that is robust to the essential hazard. The AFSMs of locally-clock proposed are described by the Extended Burst-Mode (XBM) specification. Unlike the local clock architectures of the literature that use latches to store states, our architecture is based on the Huffman's architecture, therefore they are feedback combinational functions. By making a comparison with the locally-clock AFSMs of the literature, we have a better performance and reduction in area.

I6 3:00 pm **An New Implementation of Quasi Delay Insensitive Combinational Digital Circuits**

Duarte de Oliveira, Orlando Verducci, Vitor Torres, Robson Moreno and Gracieth Batista

The asynchronous paradigm presents interesting features aiming at solving critical requirements, which demands a design of contemporary digital circuits, such as power consumption, robustness, performance, etc. A class of the asynchronous paradigm is the so called QDI (Quasi Delay Insensitive) circuits that can also be used for critical requirements design. QDI circuits are interesting for critical applications because they are robust to noise, to temperature variations, supply voltage variation, and having also low electromagnetic emissions. The main feature of QDI circuits is that they operate correctly regardless of the delay of gates, which allows a very simplified timing analysis. QDI combinational circuits are designed as a block of functions whose indicability shows the robustness of the circuit communication with the environment. This paper presents two architectures based on basic gates and an approach to the synthesis of the QDI functions blocks. The two new architectures were tested for a case study and compared with the main architectures. Our proposal shows respectively an average gain of 12%, 41.3%, 53.6% and 41.9% in time of latency, number of LUTs and power dynamic and static respectively.

POSTER SESSION 1

Tuesday, February 26, 3:20 pm
Session Chair:

C3 3:20 pm **A Simplified Tool for Testing of Feature Selection and Classification Algorithms in Motor Imagery of Right and Left Hands of EEG Signals**
Giovanna Bernardi, Tales Pimenta and Robson Moreno

Some algorithms or a combination of them are more appropriated than others depending on the type of data that is being analyzed and what features and parameters are being used. In the analysis of motor imagery (MI) in an offline EEG-based brain-computer interface (BCI), different codes with different parameters are often used, making it harder to compare the effects of the algorithms applied. In this paper, we propose a simplified and limited tool that aims to aid in the testing of feature extraction, selection and classification algorithms separately or combined for the analysis of motor imagery in offline EEGbased brain signals while providing some information about the intermediate steps of a BCI construction. A known data set is used in order to ease the comparison between other researches. Only data from channels C3, Cz and C4 are used and the MI of left hand and right hand are analyzed. The data is filtered using a band-pass Chebyshev type II filter between 5 and 35Hz. Then, The rhythms mu and beta are isolated using a discrete wavelet transform (DWT) algorithm with a db4 mother wavelet of level 5. The proposed system has two outputs: the coefficients of the DWT related to the rhythms mu and beta; and a feature vector with three chosen features that can be used as an input to a classifier. The features extracted are mean, variance and energy. These are simple but effective features. Fixing some of the parameters simplifies the tool, offers a better environment for comparison of algorithms and allows the user to focus on specific steps of a BCI construction such as the feature selection and the classification phases.

C5 3:20 pm **High-Performance Fault Diagnosis Schemes for Efficient Hash Algorithm BLAKE**
Mehran Mozaffari Kermani, Siavash Bayat Sarmadi, A-Bon Ackie and Reza Azarderakhsh

Augmenting the security of cryptographic algorithms by protecting them against side-channel active attacks (and natural faults) is essential in cryptographic engineering. BLAKE algorithm is an efficient hash function which has been developed based on Bernstein's ChaCha stream cipher. Because of the fact that Google has chosen ChaCha along with Bernstein's Poly1305 message authentication code as a replacement for RC4 in TLS for Internet security, BLAKE's implementation is of paramount importance. In this paper, we present high-performance fault detection schemes for BLAKE. Specifically, for the round function, two fault diagnosis approaches are developed and analyzed in terms of error detection capability and overhead. Through our injection-based error simulations, we show that the error coverage of almost 100% can be achieved for the proposed approaches. In addition, through hardware platform benchmarks, we show that the proposed architectures have implementations which reach acceptable area/delay overheads. The proposed high-performance fault diagnosis approaches will make the hardware implementations of BLAKE more reliable.

C7 3:20 pm **4D Bidirectional Lattice Digital Filters**
Minas T. Kousoulis, George Antoniou and Constantine Coutras

A four-dimension (4D) bidirectional digital filter, having a minimum number of delay elements, is presented. This filter, besides having a minimum number of delay elements, also has an absolutely minimal state-space vector. Furthermore the transfer function, of the proposed 4D filter, is characterized by the all-pass property as in the well known classical one-dimension (1D) case. Four-dimension and two-dimension (2D) low-order examples are provided to show the features of the circuit and state-space realization structures.

C16 3:20 pm **A Signal Reconstruction Technique For Power Delivery Analysis**
Carlos Franco, Ricardo Astro and Daniel Garcia

This document describes a signal processing technique to reconstruct the high-frequency current of a DDR4 DIMM at BGA level, by using the current measured at a remote shunt

resistor. Simulation results using the reconstructed current show very good correlation with experimental data, proving that the proposed approach is an accurate, reliable low-cost low-complexity characterization technique.

C26 **Development of Foundation Fieldbus H1 Controller IC**
3:20 pm Thiago Mussolini, Filipe Ramos, Robson Moreno and Tales Pimenta

This work proposes a Foundation Fieldbus Controller ASIC peripheral device that can provide interface to CPU/MCU. The implemented circuit satisfies the high performance requirements of equipment for industrial networks, according to IEC 61158-2. The circuit consists of Manchester encoder/decoder, time-critical hardware timers and other functions necessary to implement the data link layer for industrial networks using Foundation Fieldbus H1 protocols. The communication between the CPU/MPU and the proposed device is conducted on I2C serial communication standard. This paper describes the main characteristics of ASIC developed. The circuit was validated on XFAB XH035 technology and can be used as an alternative to commercial models that work with the old parallel ports that are leaving the market.

C29 **Optimized Fault-Tolerant Buffer Design for Network-on-Chip Applications**
3:20 pm Alan Pinheiro, Jarbas Silveira, Daniel Tavares, Felipe Silva and Cesar Marcon

Newest technologies of integrated circuits manufacture allow billions of transistors arranged in a single chip, which requires a communication architecture with high scalability and parallelism degree, such as a Network-on-Chip (NoC). As the technology scales down, the probability of Multiple Cell Upsets (MCUs) increases, being Error Correction Code (ECC) the most used technique to protect stored information against MCUs. NoC buffers are components that suffer from MCUs induced by diverse sources, such as radiation and electromagnetic interference. Thereby, applying ECCs in NoC buffers may come as a solution for reliability issues, although increasing the design cost and requiring a buffer with higher storage capacity. This paper proposes an optimized buffer using a low-cost ECC to deal with MCUs and enhance the protected information storage, pursuing to reduce the area and power required for ECC implementation. We guide the optimized buffer evaluation by measuring the fault tolerance efficiency, buffer area, power overhead and performance of the proposed technique. All tests included the comparison with a non-optimal appliance of ECC in a NoC buffer. The results show the proposed technique reduces the area and power overhead in buffers with ECC and allows a considerable fault tolerance against MCUs with a small performance impact.

C46 **A Digital Random Number Generator Based on Irregular Sampling of Regular**
3:20 pm **Waveform**
Burak Acar and Salih Ergün

There is an increasing demand for the security of information over the past few decades. Random Number Generators (RNGs) play a significant role in many cryptographic applications for generating unpredictable bit-streams. Despite the fact that Application Specific Integrated Circuit (ASIC) implementation of RNGs are usually preferred for their high performance, fully digital circuits implemented on Field Programmable Gate Array (FPGA) platforms are more attractive for designers considering their ability of rapid-reconfigurable prototyping, and their easy integration to other digital circuits. In this study, a new improvement based on irregular sampling of regular waveform is proposed for ring oscillator based RNGs. It is subjected to National Institute of Standards and Technology (NIST) 800-22 test suite and it passes full tests without any post-processing. An attack circuit is also implemented to see the robustness of the designed RNG against coupling-based attacks. No effective correlation can be obtained between the outputs of the target and the attack circuit; in spite of, their extremely close placement to each other inside the FPGA chip. The feasibility of the proposed method is given in experimental results.

C55 **A Tools Flow for Synthesis of Asynchronous Control Circuits from Extended**
3:20 pm **STG Specifications**
Higor Delsoto, Duarte de Oliveira, Gracieth Batista, Diego Silva and Leonardo Romano

Asynchronous control circuits are very important in heterogeneous systems, existing two different specifications previously proposed to describe the asynchronous controls: the signal transition graph (STG) and the extended burst mode (XBM). These specifications, despite being quite popular, present certain limitations in describing some interfaces for heterogeneous systems. In this paper, we propose a flow of tools for the automatic synthesis of asynchronous control circuits, which are described by the specification called Extended Signal Transition Graph (XSTG) that has all features of STG and XBM specifications. For a set of benchmarks, the XSTG description shows in addition to a natural ability to describe conditional signals, a high compaction, in the case an average reduction of 54.3% in places and 47.4% in transitions, when compared with STG specification.

8:30 am **Keynote: End of CMOS miniaturization and technology development after that**

Wednesday, February 27, Uruma Room

Hiroshi Iwai
Tokyo Institute of Technology, Yokohama, Japan

Recent smart society has been conducted by the progress of semiconductor technologies, especially by that of CMOS miniaturization. However, it is afraid that the CMOS miniaturization will reach its limit substantially in several years. However, semiconductor technology development will continue in future after that. In this talk, the limit of the CMOS miniaturization is explained and the semiconductor device technology development after reaching the scaling limit is discussed.

POSTER SESSION 2

Wednesday, February 27, 9:30 am
Session Chair: J. Marín

C76 **About Performance Faults in Microprocessor Core in-field Testing**
9:30 am Julio Perez Acle, Ernesto Sanchez and Matteo Sonza Reorda

When microprocessor-based devices are used in safety-critical applications (e.g., in automotive systems), it is common to adopt solutions aimed at testing them in-field, so that permanent faults that may affect them are identified before they cause critical consequences. In this way, the required reliability figures can be achieved. A popular solution to perform in-field test (especially when executed concurrently to the application) is based on triggering the execution of proper procedures (composing a Self-Test Library, or STL), which are able to activate faults and make them visible when checking the produced results (e.g., in memory). Unfortunately, a special class of faults exists (named Performance Faults), which do not impact the value of the results, but only the timing behavior of the processor. This paper describes a set of experiments aimed at quantitatively evaluating the number of these faults in a simple processor core, and outlines some solutions that can be used for their detection.

C77 **On UVM Reliability in Mixed-Signal Verification**
9:30 am Wilmer Ramirez, Héctor Gómez and Elkim Roa

During the last decade, Universal Verification Methodology (UVM) has become a popular standard test methodology for verification of intellectual property (VIP) within digital and mixed-signal systems. UVM prominent features include stimulus automation, I/O checking and code reuse. This paper analyzes the strengths and weaknesses of UVM along with measurements of reliability using a 32-bit LPDDR3 memory interface and a bandgap voltage reference. Simulation results indicate that reliability is limited by complexity of the circuit under test and proper UVM setup to get considerable analog simulation coverage. For analog cases, UVM-AMS can render low reliability considering that a common practice in analog design is creating

multiple testbenches according to the function/domain tested. VIP by itself should be used as a complement to traditional verification practices even when assuming access to a fully detailed UVM-AMS VIP.

C79 **Resilient Hardware Design for Critical Systems**
9:30 am Marcos Farias, Nadia Nedjah and Paulo Victor Carvalho

With the constant breakthroughs in technology components, there has been an increase in the capacity and performance of FPGA. Nevertheless, new methods to keep fault tolerance at an appropriate level for critical applications in hardware must be considered, particularly due to the transient nature of some radiation-induced faults. The most commonly used methods to mitigate these faults involve redundancy, such as the Triple Modular Redundancy (TMR) with the 2 out of 3 voter solution (2oo3), the most common passive method, in addition to active methods, such as the replacement of resources allocated a priori or dynamic recovery. The objective of this study is to propose a hardware architecture that increases the reliability in the use of circuits implemented in FPGAs, in addition to the one found in circuits with TMR, but without significant increase the area required by the redundant solution. The proposed solution uses comparators, a state machine-based controller and a multiplexer module to operate an architecture with three redundant modules and a spare one. The analysis shows that the proposed architecture is more reliable and keeps this reliability for longer periods of time than redundant solutions that use more area, such as the 3 out of 5 configuration (3oo5).

C94 **A Very Compact CMOS Analog Multiplier for Application in CNN Synapses**
9:30 am Antonio Jose Sobrinho De Sousa, Fabian de Andrade, Gabriele Goncalves, Ana Isabela Araújo Cunha, Edson Pinto Santana, Fernando Martins Cardoso and Kelvin Kéfren Carvalho Feitosa Nunes

This work presents a CMOS analog multiplier architecture for application as the synapse of analog cellular neural networks. The circuit comprises two voltage-mode inputs and a current-mode output. Simulated performance features include: input voltage range of +100 mV, 23 uW static power, maximum total harmonic distortion of -32 dB and -3 dBbandwidth of 51.2 kHz. The active area totalizes only 40 um2.

C105 **Low-Power and High-Throughput Approximate 4x4 DCT Hardware Architecture**
9:30 am Mateus Leme, Luciano Braatz, Daniel Palomino, Marcelo Porto and Luciano Agostini

Mobile devices with multimedia processing capabilities are becoming more and more present, despite their energy restrictions. On the other hand, multimedia applications are very demanding tasks, which have a negative impact on the battery lifetime of mobile phones. Nonetheless, video encoding, one of the most demanding multimedia applications, can benefit from approximate computing to save energy. This paper proposes an approximate 4x4 Discrete Cosine Transform (DCT) hardware architecture using the imprecise Lower Part-OR Adder (LOA). The imprecise operators, such as LOA, are one of many approaches to approximate computing. This approximate hardware architecture is developed with different imprecision levels. The presented approximate 4x4 DCT hardware architecture synthesis results show area reduction up to 13.6%, power savings up to 23% and throughput increase up to 26.45% while having a negligible to small BD-Rate impact.

C116 **Delta-Sigma modulated output temperature sensor for 1V voltage supply**
9:30 am Jose Ramirez, João Tiol, Fabiano Fruett and Diego Deotti

This work presents a temperature sensor with a digital Sigma-Delta modulated output designed to work at a supply voltage as low as 1V to operate in a temperature range from -25oC to +100oC. A Bandgap current reference circuit generates a current proportional to the temperature I_PTAT and a reference currentI_REF. Both currents are integrated in a capacitor within a Delta-Sigma modulator, resulting in a digital output whose average value is proportional to the temperature. The sensor was designed using 180nm TSMC technology and occupies an area of 540um×500um. Simulations showed a linear output response and a duty cycle variation of 0.52% per Celsius and a 180µW power consumption.

C119 **A 130 nm CMOS LNA for Satellite Application**
9:30 am Renê Timbó, Hamilton Klimach and Eric Fabris

This work presents the design of a narrowband Low Noise Amplifier (LNA) that is a part of a transponder project of a UHF satellite for the Brazilian Environmental Data Collecting System (SBCDA). The proposed LNA operates at 401.635 MHz moreover, it provides 28dB of Power gain, 3.6dB of noise figure (NF), IIP3 of -28 dBm and 6.53 mW of Power consumption and it was designed in a standard 130 nm CMOS process.

10 am PARALLEL SESSIONS

Wednesday, February 27

Session 5-1: LASCAS - Digital Circuits and Systems
Wednesday, February 27, 10:00 am, Uruma Room
Session Chair: S. Eslava

C66 **A Sub- µW Reconfigurable Front-End for Invasive Neural Recording**
10:00 am José Luis Valtierra, Rafaella Fiorelli, Manuel Delgado-Restituto and Angel Rodriguez-Vazquez

This paper presents a sub-microwatt ac-coupled neural amplifier for the purpose of neural signal sensing. A proposed reconfigurable topology embeds in it filtering capabilities allowing it to select among different frequency bands inside the neural signal spectrum. Power consumption is optimized by designing for bandwidth-specific noise targets that take into account the spectral characteristics of the input signal as well as the noise bandwidths of the noise generators in the circuit itself. An experimentally verified prototype designed in a 180nm CMOS process draws 803nW from a 1V source. The measured input-referred spot-noise at 150Hz is 130nV / Hz while the integrated noise in the 200Hz-5kHz band is 3.6µV rms.

C78 **Framework for Heterogeneous Many-core SoCs Generation**
10:20 am Marcelo Ruaro, Luciano L. Caimi, Vinicius Fochi and Fernando G. Moraes

This work presents a framework for heterogeneous many-core SoCs generation, which comprises a flexible EDA framework and a many-core model for heterogeneous SoCs. The framework together with the many-core model supports the integration of processors, network interfaces, routers, and peripherals. The hardware model is cycle-accurate, with a SystemC model to speed up simulation time and a VHDL model enabling prototyping in FPGAs devices. The framework provides a rich set of graphical debugging tools enabling an easy and intuitive understanding of computation and communication events happening at runtime. The coupled integration of the platform model to the EDA framework makes the many-core well suited to be employed in research and teaching. As case-study, we provide an evaluations addressing the many-core generation, simulation, and debugging.

C85 **A High Throughput Hardware Architecture Targeting the AV1 Paeth Intra Predictor**
10:40 am Marcel Corrêa, Bianca Waskow, Jones Goebel, Daniel Palomino, Guilherme Corrêa and Luciano Agostini

AV1 is an open-source and royalty-free video coding format, which was developed by the AOMedia industry consortium and released in June 2018 as the state-of-the-art in video coding. The main goal of AV1 development was to achieve substantial compression gain over high-performance codecs such as VP9 and HEVC, while keeping a practical decoding complexity, hardware feasibility and its open and free status. This paper presents a highly parallelized hardware architecture for the AV1 Paeth intra predictor supporting all 19 block sizes allowed, capable of processing UHD 4K videos at 120 frames per second. When synthesized to the TSMC 40nm cell library targeting a frequency of 315MHz, the proposed design used 247.28K gates and showed a power dissipation and an energy efficiency of 268.36mW and 179.74pJ/sample respectively.

C98 **A Low-Area Direct Memory Access Controller Architecture for a RISC-V Based**
11:00 am **Low-Power Microcontroller**
Abstract
Hanssel Morales, Ckristian Duran and Elkim Roa

In this work, we present a low area DMA controller that enables low-cost SoCs where subsystems need constant memory access. Small interfaces and a unique FIFO handling read/write transactions are fundamental blocks in this design. As proof of concept, the testing system also includes a RISC-V RV32IM processor, a USB 1.1/2.0 PHY and a QSPI interface. We implemented a whole microcontroller using a TSMC 0.18um technology node, where the DMA occupies 4.2% of the total area. The results show a total DMA area of 1997 gates using 4 information channels, which is 70% smaller area in comparison with recent low-area DMAs.

C111 **FPGA IP for Real-time 4K HDR Image Decoding on VR Devices**
11:20 am Kamalavasan Kamalakkannan, Natheesan Ratnasegar, Pradeep Kathirgamaraja, Gowthaman Sivakumaran, Aravinth Sivakaneshan and Ajith Pasqual

Quad High Definition (QHD/4K) Virtual Reality (VR) Headsets with High Dynamic Range (HDR) technology will provide a superior experience to users. Wireless VR headsets are attractive as it offers freedom on mobility and higher user comfort. Cloud and workstations are capable of rendering 4K HDR scenes in real-time. A compression standard based encoding is required for the efficient transmission of these scenes through wireless networks. Decoding 4K HDR frames at VR devices in real-time is a challenge. Hardware decoders are power and memory efficient than software-based solutions. In this paper, we are proposing JPEG XT - Profile C based hardware architecture to decode 4K HDR frames in real-time. In this work, we are employing novel methods of merged base and residual layer decoding pipelines, probability-based hybrid Huffman lookup table architecture designing and sparsity aware inverse zig-zag processing. Our decoder is implemented in Xilinx VC707 board and achieved the decoding performance of 4K HDR frames at 30fps while consuming only 7K of LUTs, 12K of Registers and 1980Kb of block memory. Single clocked architecture, use of clock enabling logic and resource sharing in time reduced power consumption to less than 1 watt.

C25 **Microprocessor Design with a Direct Bluetooth Connection in 45 nm Technology**
11:40 am **Using Microwind**
Esteban Garzon, Félix Chavez, Diego Jaramillo, Luis Sánchez, Sofía Lara, Carlos Macías, Eliana Acurio, Luis-Miguel Procel-Moya, Lionel Trojman and Etienne Sicard

This paper presents the full-custom design of a 45 nm microprocessor using the electronic design automation (EDA) software, Microwind. The design consists of fundamental modules: the arithmetic logic unit (ALU), memory, counter and an integrated Bluetooth (BT) port working at the 2.4 GHz. This design is validated by simulation under a process, voltage, and temperature (PVT) testing. The microprocessor can handle up to 4 bit since its purpose is focused on specific applications such as the internet of things (IoT). In order to communicate to the external world and with other devices, a strong input/output data interface and radio frequency (RF) transmission modules are implemented. Moreover, the RF module also contains a Bluetooth communication, which allows the wireless data transmission from/to the microprocessor.

Session 5-2A: LASCAS - Sensory Circuits and Systems
Wednesday, February 27, 10:00 am, Pamba 1 Room
Session Chair: C. Silva

C15 **ISFETs: theory, modeling and chip for characterization**
10:00 am Rodrigo Wrege, Márcio Schneider, Janaina Guimarães and Carlos Galup-Montoro

The ISFET (Ion Sensitive Field Effect Transistor) is a structure based on the MOSFET (Metal Oxide Field Effect Transistor) which is capable of measuring ionic concentration of a solution.

The ISFET has been used for such areas as DNA sequencing, viruses and bacteria detection. The basic idea behind the ISFETs emerged in 1970, but a deeper understanding of some of its non-idealities and the development of architectures to reduce their effects are still needed. For that reason, this work revisits the basic principles of ISFET operation. The ISFET modeling using the binding site theory, Gouy-Chapman-Stern model and the Advanced Compact Model of the transistor is introduced and implemented in Matlab®. Furthermore, the details of a chip designed on the Virtuoso® platform, aimed at characterizing the ISFETs on the SilTerra D18V technology, are presented. Simulation results estimate an average sensitivity of 45.3 mV/pH for the designed devices over a pH range from 1 to 10. The chip sent for fabrication was kindly supported by Chipus Microeletrônica S.A. and SilTerra Malaysia Sdn Bhd.

Session 5-2B: LASCAS - Communications Circuits and Systems
Wednesday, February 27, 10:20 am, Pamba 1 Room
Session Chair: N. Calazans

C113 10:20 am **Smart Water Management System using the Microcontroller ZR16S08 as IoT Solution**
Michel Machado, Tiago Junior, Michele Silva and João Martins

This paper presents a smart water management system using the microcontroller ZR16S08 as IoT solution, for water distribution support and losses prevention. The system operates through the smart monitoring of the water flow in pipes of the water distribution network, aiming to ensure quality of the water supply, knowing that water losses characterize one of the great problems in the world, as pipe holes may be open doors to water contaminants. As an alternative to circumvent this issue, a series of experiments were taken to create a network of sensors capable of monitoring water pipes in real time. Adopting criteria such as low consumption and low cost, the use the ZR16S08 microcontroller in the design of wireless sensor nodes that will be coupled in the water pipes was adopted. Complementing the system, a central processing unit, composed of a Raspberry Pi microcomputer, manages the traffic of the information collected by the sensor nodes and routes it to a web server. All data addressed by the central unit are available on-line by means of a supervisory platform. Considering the size of the sensor nodes, their power consumption, and regulatory issues, a link between the sensor nodes, operating at a frequency of 433MHz, was defined. Preliminary results show the effectiveness of the proposed architecture for sensor nodes, allowing application for the monitoring of water and controlling losses.

C117 10:40 am **A Programmable and Low-Area On-Die Termination for High-Speed Interfaces**
Luisa Dovale, Juan Sebastian Moya and Elkim Roa

Although much progress has been made over the years in high-speed I/O, there is no comprehensive characterization of their termination design. In contrast to the widespread notion that a programmable termination might not offer any challenge, electromigration in conjunction with ESD compliance and programmability demand considerable attention during the termination design. Here we combine a design methodology and circuit techniques to address the hinted challenges. Overall, our study provides a comprehensive characterization on the design of a 35W-to-65W matching network. As a result, this paper presents a programmable ESD-compliant on-die termination occupying an area of 0.03mm2 on a standard 180nm CMOS with a maximum worst case of 7.14mA static current consumption.

C10 11:00 am **Dedicated monitoring service without routing mitigation for Networks-on-Chip**
Gabriel Ganzer and Marcelo Daniel Berejuck

We present the design and evaluation of a non-intrusive packet delivery monitoring service on a Network-on-Chip (NoC) that focus real-time systems-on-Chip (SoC). Recent works show that using adaptive routing or optimization techniques are solutions to improve its latency. These strategies usually need to know the traffic behaviour previously to make changes. A monitoring service is indicated as a solution to this issue, but since silicon consumption is a restriction in these projects, most of them use routers or other NoC's resources to performer such task. Our design is based on a strategy that does not interfere with the NoC operation to collect and to evaluate traffic information.

C13 11:20 am **Analog-to-Information Converter Based on Off-the-Shelf Components and SoC-FPGA**

Alexander López-Parrado, Alexander Vera-Tasamá, Juan F. Medina-Lee and Duvier D. J. Bohórquez-Palacio

This brief presents design and implementation of a 100-MHz Analog-to-Information Converter (AIC) based on Random Demodulator (RD); for this purpose, we used off-the-shelf components to implement the analog front-end and a SoC-FPGA chip to implement the digital hardware/software sub-system. Analog front-end is composed of one mixer and one low-pass filter, which were implemented by using a Gilbert Cell and a passive RC circuit, respectively. Hardware/software sub-system was implemented on the Field Programmable Array (FPGA) and Hard Processor System (HPS) sides of the SoC-FPGA chip, were FPGA side was used to implement the hardware that manages RD and HPS side was used to implement spectrum recovery algorithms. Finally, verification results showed that designed AIC can recover sparse signals of 100 MHz bandwidth, where a sub-Nyquist rate of 4 MHz is used along with two Compressive Sensing (CS) recovery algorithms.

C18 11:40 am **A Black-box Model for Neurons**

Nestor Roqueiro, Carlos Claumann, Antoni Guillamon and Enric Fossas

We explore the identification of neuronal voltage traces by artificial neural networks based on wavelets (Wavenet). More precisely, we apply a modification in the representation of dynamical systems by Wavenet which decreases the number of used functions; this approach combines localized and global scope functions (unlike Wavenet, which uses localized functions only). As a proof-of-concept, we focus on the identification of voltage traces obtained by simulation of a paradigmatic neuron model, the Morris-Lecar model. We show that, after training our artificial network with biologically plausible input currents, the network is able to identify the neuron's behaviour with high accuracy, thus obtaining a black box that can be then used for predictive goals. Interestingly, the interval of input currents used for training, ranging from stimuli for which the neuron is quiescent to stimuli that elicit spikes, shows the ability of our network to identify abrupt changes in the bifurcation diagram, from almost linear input-output relationships to highly nonlinear ones. These findings open new avenues to investigate the identification of other neuron models and to provide heuristic models for real neurons by stimulating them in closed-loop experiments, that is, using the dynamic-clamp, a well-known electrophysiology technique.

Session 5-3A: LASCAS - EDA

Wednesday, February 27, 10:00 am, Pamba 2 Room

Session Chair: E. Sanchez

C54 10:00 am **Mapping and Placement in NoC-based Reconfigurable Systems Using an Adaptive Tabu Search Algorithm**

Guilherme Apolinário Silva Novaes, Luiz Carlos Moreira and Wang Jiang Chau

Mapping and Placement still are big challenges in Networks-on-Chip (NoCs) design, due to the scalability, although several heuristics have been proposed to solve them. These problems belong to the class of Quadratic Assignment Problems (QAP). For NoC-based dynamically reconfigurable systems (NoC-DRSs), both mapping and placement problems present an additional complexity level due the reconfigurable layers/scenarios, being treated only by Genetic Algorithm meta-heuristics; however, several researches have described Tabu Search meta-heuristics as the best QAP solvers. This paper presents formalization for the mapping and placement on 2D-Mesh FPGA NoC-DRSs, and provides as solver, a novel approach of adaptive Tabu Search, named Nav-adaTS. Results with a series of benchmarks are presented and compared to a basic adaptive Tabu Search and to the genetic algorithm implementation.

C19 10:20 am **Clip Clustering for Early Lithographic Hotspot Classification**

Andre Oliveira, Julia Puget, Carolina Metzler and Ricardo Reis

Early lithography hotspot detection is critical to improve manufacturing yield. EDA tools have been proposed to detect potentially problematic patterns during physical design and physical

verification stages. Considering that detailed lithography simulation has a high computational cost for full-chip scale, the pattern matching method proved to be a fast solution with good accuracy due to a set of pre-characterized patterns as input. We propose a clip clustering method for pattern classification in early detection of lithography hotspots. We focus at both clip representation and clip clustering stage that is the major challenge of this method. We perform experiments on 2016 ICCAD contest benchmark suite and results show the efficiency of our clustering approach. The algorithm supports both area and edge constrained clustering. Our solution generates on average 9.4% fewer clusters than the contest winner while staying within 16% range on average from the state of the art algorithms. Moreover, Our clustering pattern-driven layout strategy outperforms the 2016 ICCAD winner on runtime by up to 60%.

C38 10:40 am **A State Assignment Method for Extended Burst-Mode gC Finite State Machines Based on Genetic Algorithm**

Tiago Curtinhas, Duarte de Oliveira, Gracieth Batista, Vitor Torres and Leonardo Romano

This paper proposes a new algorithm for state assignment of Extended Burst-Mode Asynchronous Finite State Machines (XBM_AFSM). The proposal is based on genetic algorithm and introduces a novel style of state assignment. It improves the results and overcomes the previous methods found in literature once it addresses the “state minimization”, the “critical race free coding” and “coverage” as a single problem. Furthermore, it is able to detect the conflicts in XBM specification and insert the minimum number of state variables in the XBM specification to eliminate those conflicts. A dedicated computational tool called SAGAAs_gC implements the algorithm and it was tested in a set of 39 XBM benchmarks. When compared to 3D tool, our method achieved an average reduction of 21.4%, 16.5% and 12.12% in the number of state variables, number of literals and transistors, respectively. Results show that the method and dedicated computational tool SAGAAs_gC achieved good and reliable results, showing a high potential of practical implementation in actual circuit designs.

Session 5-3B: IBERCHIP

Wednesday, February 27, 11:00 am, Pamba 2 Room

Session Chair:

I7 11:00 am **Architecture for Low-Power Gated-Clock Synchronous FSMs Operating on Double-Edge Clock**

Duarte de Oliveira, Diego Silva, Gracieth Batista and Leonardo Romano

Today a number of digital systems are described by an architecture consisting of a network of synchronous FSMs (finite state machines) with data-paths. These are battery-fed and maybe implemented in VLSI technology. Since the batteries must have long life, reduction of energy consumption is the most important task in the design of such systems. In order to reduce dissipated power, a number of strategies have been proposed in the literature for both synchronous FSMs and data-paths. For synchronous FSMs, there are two interesting strategies for to reduce consumption: 1) clock logic control that inhibits clock in self-transitions and is turned towards single-edge triggered flip-flop; 2) synchronous FSMs operating with double-edge triggered flip-flops (DET-FFs). In this paper, we propose target architecture for synchronous FSMs that use output signals as state signals, have clock logic control and operate with DET-FFs. This architecture allows drastically reducing clock signal activity. Comparing the proposed architecture with different implementations of synchronous FSMs for case study was obtained an average reduction of 39.4% in the dynamic power.

I10 11:20 am **An Implementation of the DES Encryption Algorithm with High Throughput using FPGA**

Diego Silva, Duarte de Oliveira, Gracieth Batista and Leonardo Romano

Currently, digital systems that are able to meet major security restrictions are increasingly being demanded, both in the military and in commercial areas. Data security can be achieved by cryptographic algorithms. An important encryption algorithm known as DES (Digital Encryption Standard) was implemented in Field Programmable Gate Array (FPGA) in different architectures. In this paper we propose an implementation of the DES algorithm in FPGA, in the

synchronous pipeline style. Comparing with different FPGA implementations of the literature and realized on different devices, the proposal achieved an average increase in throughput of 110.9%.

Session 5-4A: LAEDC - Devices and materials
Wednesday, February 27, 10:00 am, Pamba 3 Room
Session Chair:

E13 10:00 am **Origin of the Negative Differential Resistance in the output characteristics of a picene-based Thin-Film Transistor**
Joaquin Puigdollers, Eloi Ros, Pablo Ortega and Cristobal Voz

In this work, we have fabricated p-type picene thin-film transistors. Although the devices exhibited good electrical performance with high field-effect mobility (up to 1.3 cm2 V−1s−1) and on/off ratios above 105, the output characteristics showed Negative Differential Resistance for higher drain-source voltage. A plausible explanation of this phenomenon is developed.

E14 10:20 am **Degradation Study of Inverted Polymer Solar Cells Using Inkjet Printed ZnO Electron Transport Layer.**
Angel Sacramento, Magaly Ramírez, Victor Balderrama, Ivan Garduño, Magali Estrada and Lluis Marsal

In this study, we analyze the stability and degradation of inverted organic solar cells (iOSCs) partially fabricated under air environment. It is compared the degradation of iOSCs manufactured with PFN against inkjet printed ZnO as electron transport layer (ETL). The active layer use PTB7 and PC70BM as donor and acceptor material, respectively for all devices. The electrical parameters during the degradation process were extracted from the current density – voltage characteristics (J–V) under light and dark conditions. The power conversion efficiency (PCE) of the devices under nitrogen without encapsulation decreased down to 80% after 58 h for iOSCs with PFN and after 189 h for inkjet printer ZnO. Photovoltaic devices under air and without encapsulation manufactured with ZnO, the PCE decrease to 80% after 160 h.

E22 10:40 am **Microfluidic sub-Terahertz sensor for on-line determination of ethanol concentration in binary liquid mixtures**
Salomão Moraes da Silva, Johan Stein and Jacobus Swart

Development of a sub-THz sensor tool coupled to a microfluidic platform for determination and control of binary liquid mixtures is reported. Contactless and on-line measurements are demonstrated for the determination of ethanol concentration and controlling by micromixer device. We have developed a label-free chemical sensing methodology coupling a sub-terahertz sensor technology in microfluidic devices fabricated on glass and polydimethylsiloxane. We demonstrated on-line sensing and control of ethanol concentration on demand. The THz-microfluidic sensing strategy represents a versatile tool for fast and easy integration in microfluidic devices, for concentration detection and linear control of binary mixtures concentration in a contactless mode using micro reactors in laminar flow and fast mixing mechanism by convection.

Session 5-4B: LAEDC - Devices physics
Wednesday, February 27, 11:00 am, Pamba 3 Room
Session Chair:

E18 11:00 am **The magnetic field impact on the 1/f noise and the charge-pumping measurements in MOSFETs**
Oscar Vicente Huerta Gonzalez, Adrian I. Tec-Chim and Edmundo Gutierrez

An investigation of the Low Frequency Noise and Charge-pumping measurements in n-MOSFETs was conducted at room temperature under the influence of perpendicular-to-the surface magnetic fields. The anomalous response of the transistor under these conditions was analyzed in detail to understand the gate oxide trapping mechanisms and its correlation to the

oxide-semiconductor interface. The analysis revealed a magneto modulation of the noise characteristic and the pumped current, possibly, as a result of the magnetic field altering the trapping dynamics.

E24 **Memristors: A perspective and impact on the electronics industry**
11:20 am Alexander Vera, Jorge Marin and Marisol Gomez

Memristors are devices that promise a great impact on the electronic industry at the level of implementation, comparable to that caused by the invention of the transistor and the integrated circuit, both based on semiconductors. These devices may contribute to the improvement of the performance in both analog and digital circuits, especially in those demanding high consumption of resources due to signal processing. Although implementation approaches based on materials such as titanium dioxide (TiO2), led by HP Labs, are available for these devices, a wide commercial adoption of this technology has not arrived yet. A large set of contributions in the last ten (10) years, including patents and academic papers, are oriented to implementation models based on simulation and emulation at different fields of the electronics industry. Among these contributions, the simulation of biological systems has been extensively studied. This paper presents an overview of the impact of the memristor on the main application scenarios in the electronics industry, from the device implementation approaches to the architectural schemes of hardware systems for specific applications based on the models and features of these devices.

E8 **Antennas Design for UHF Passive RFID Tags**
11:40 am Jorge Daniel Terán Guerra, Jaime Martínez Castillo and Raul López Leal

There are many different applications for RFID tags, each one related to the way they are designed. In this document we present the basics to design antennas for UHF-RFID passive tags using some miniaturization techniques and inductive coupling. Also, we show the importance of the antenna parameters and the methodology for design our own antenna in a few steps using the methods explained in this work.

2 pm PARALLEL SESSIONS

Wednesday, February 27

Session 6-1: LASCAS - Digital Circuits and Systems
Wednesday, February 27, 2:00 pm, Uruma Room
Session Chair: R. Reis

C61 **Analytical Modeling of Chaotic Sampling of Regular Waveform for Random Number Generation**
2:00 pm Kaya Demir and Salih Ergün

In this paper, an analytic approach is taken towards the analysis of a class of true random generators where an irregular square wave generated by a continuous-time chaotic oscillator and a comparator structure is used to sample a regular continuous-time waveform. Numerical and analytic equations for probability distribution have been derived for D flip-flop topology. Kernel density estimation method is utilized to describe bit distribution in the output. Then random bits are generated using analytical formulas and results from numerical simulations. Using the concepts of auto correlation and approximate entropy, the relationship between the regular and the chaotic waveform frequencies needed to generate uncorrelated bit stream have been investigated.

C81 **Asynchronous Quasi-Random Number Generator: Taking Advantage of PVT Variations**
2:20 pm Rodrigo Wuerdig, Marcos Sartori and Ney Calazans

Random number generators find application in many fields, including cryptography, digital signatures and network equipment testers, to cite a few. Two main classes of generators are

ususally proposed as hardware implementations, pseudo-random number generators and true number random generators. The former are simple to build and use, but cannot be used in every application specially those where randomness is meant to support security. The later can be complicated to build, since they often must rely on hard-to-predict events that can rarely be produced in the deterministic world of digital circuits. This work proposes a quasi-random number generator hardware implementation, intended to provide most of the benefits of true number random generators with costs closer to those of pseudo-random number generators. The quasi-random number generator described here relies on the use of asynchronous circuit design techniques allied to process, voltage and temperature variability to achieve relatively high degrees of randomness. An FPGA prototype demonstrates the feasibility of the approach.

C101 **Accelerating Template Matching for Efficient Object Tracking**
2:40 pm Alexandre De Vasconcelos Cardoso, Nadia Nedjah and Luiza De Macedo Mourelle

Template matching is used to determine the degree of similarity between two images of the same size. Pearson's Correlation Coefficient is applied, due to its property of invariance to brightness changes. This coefficient is computed for each image pixel, entailing a computationally intensive task. In order to accelerate this process, a dedicated co-processor was designed to implement this computation. To improve the search for the maximum correlation point between the image and the template, we used, in this work, Bacteria Foraging Optimization, one of the swarm intelligence strategies. The search process is run by an embedded general purpose processor. The work presented in this paper describes the implementation of the embedded system and compares the results obtained here to those previously obtained when using other swarm intelligent strategies.

Session 6-2: LASCAS - Communications Circuits and Systems
Wednesday, February 27, 2:00 pm, Pamba 1 Room
Session Chair: L. Trojman

C43 **A Dependency-Free Real-Time UHD Architecture for the Initial Stage of HEVC**
2:00 pm **Motion Estimation**
Haris Chaudhry Mendívil, Mario Andres Raffo Jara, Carlos Silva-Cardenas and Ernesto Cristopher Villegas Castillo

Novel coding tools and algorithms were proposed in the High Efficiency Video Coding Standard (HEVC), and are still being proposed over the HM reference software in order to achieve a better compression efficiency, decrease encoding time, make its stages suitable for hardware implementation, and other independent improvements. Particularly, for the initial stage of the motion estimation (ME) process, the Advanced Motion Vector Prediction (AMVP) and the Dynamic Search Range (DSR) algorithms were introduced in the field targeting the determination of the motion vector predictor (MVP), also used as the search center, and search range (SR), which are parameters needed in the subsequent steps of ME. However, the significant complexity of these new tools enhances the need to develop hardware (HW) accelerators. Furthermore, in the field of HW architectures for video compression, techniques that solve dependency problems (which are detrimental to performance) —in this case, between sub-stages of ME— were proposed by some authors. Thereupon, an integrated and synchronized dependency-free HW architecture for the initial stage of the ME process —regarding MV prediction and SR calculation— is proposed in this paper. Synthesis results on a middle ground FPGA (Kintex-7 xc7k70tfbv676-1) show that the integrated architecture can achieve a throughput up to 8K at 72 frames-per-second (4:2:2 subsampling) while using a maximum of 7.04% of the FPGA resources (on slice LUT's).

C80 **A Novel Model for the Resonance Frequency in Lamb Wave Resonators based**
2:20 pm **on AlN**
Andres Felipe Jaramillo Alvarado, Francisco Javier De la Hidalga Wade, Alfonso Torres Jacome and Emmanuel Torres Rios

Current multiplexers, oscillators and active filters, commonly based on active devices, are fundamental components of any communication system, nevertheless, their performance is

limited by the power consumption. Due to the high requirements in modern communication systems, the new topologies and the optimized design of each basic component must be a main issue to investigate. The piezoelectric resonators are passive devices that can replace some active components in oscillators and active filters. This work presents a novel model for the resonance frequency of any type of piezoelectric resonator. As a particular case, we use this in a Lamb Wave Resonator (LWR) with aluminum electrodes and Nitride Aluminum (AlN) as the piezoelectric layer. The experimental validation of the model was conducted using an LWR designed and fabricated at the INAOE's facilities. The measured S parameters delivered a resonance frequency of 541 MHz; and this result was compared to that predicted by the proposed model, showing a relative error of 5.4%, which is much lower than the 18.8% obtained by using the standard design methodology.

C91 2:40 pm **A Pseudo-Raised Cosine IR-UWB pulse generator with adaptive PSD using 130nm CMOS process**

Luiz Carlos Moreira, José Fontebasso Neto, Walter Silva Oliveira, Thiago Ferauche and Guilherme Apolinário Silva Novaes

This paper presents the design of a Pseudo-Raised Cosine Impulse Radio Ultra-Wide Band (IR-UWB) pulse generator with adaptive PSD (Power Spectrum Density) that produces pulse shaping just altering the number of oscillations and amplitude. The complete pulse generator circuit is composed of 11 blocks of edge combiner stages implemented with high impedance circuits each, a digital control block, and a filter. This circuit can generate from four to eleven oscillations per clock edge to compose a PRC (Pseudo-Raised Cosine) at the output. The proposed circuit operates at about 10.3 GHz and generates three basic pulses, with a range of 10, 20 and 30 mV and four other amplitude combinations. The post-layout simulations were performed using the Cadence Spectrum/Virtuoso, and the dynamic energy varied from 5.02 fJ with four oscillations to 16.11 fJ with eleven oscillations per pulse, respectively. Thus, the maximum PSD peak is -60 dBm, the minimum is -72 dBm with a voltage supply of 1.2 V. Finally, the Pulse Repetition Frequency (PRF) of 100 MHz and the size of the main chip occupies an area of 0.042 mm2 (without pads).

Session 6-3: LASCAS - Power and Energy Circuits and Systems
Wednesday, February 27, 2:00 pm, Pamba 2 Room
Session Chair: C. Silva

C51 2:00 pm **An Implementation of Extended Burst-Mode Specifications as Quasi Delay Insensitive State Machines**

Duarte de Oliveira, Orlando Verducci, Vitor Torres, Gracieth Batista, Robson Moreno and Leonardo Romano

Due to the increasing demand for mobile devices, the search for ultra-low-power projects is becoming a priority. One technique that allows a strong reduction of circuits dissipated power is the sub-threshold voltage operation, but it leads to some drawbacks. The QDI (Quasi Delay Insensitive) asynchronous circuits class shows to be an interesting solution to these problems, when compared to synchronous circuits and in CMOS-UDSM (Ultra Deep Sub-Micron) technology. Asynchronous finite state machines (AFSMs) are important components in a QDI asynchronous system. This paper proposes a new architecture and a synthesis method for QDI AFSMs described in Extended Burst-Mode (XBM) specification. The architecture and synthesis method are presented through case study. The QDI_XBM_AFSM proposed presents for four benchmarks an average reduction of 17.7%, 29.2% and 37.8%, respectively, latency time, dynamic power and static, when compared with five QDI AFSMs of the literature.

C39 2:20 pm **On Chip Solar Energy Harvesting System Using Substrate Diode PV Cell and Fractional Open Circuit Voltage MPPT Implementation**

Daniel Rodriguez, Carlos Bernal and Guillermo Serrano

This work presents a power management architecture for an On-Chip solar energy harvesting system applied to low power applications. A functional Power Management Circuit with MPPT was designed using a 0.13 um CMOS technology, to provide an output voltage of 1.2 V by using

just one external inductor that can be co-packaged with the IC. The proposed fractional open circuit voltage MPPT circuit, along with the DC/DC converter controller, allows the system to achieve efficiencies of up to 81%. Such high efficiency was achieved via a self-synchronize diode and a negative level shifter reducing drastically the power losses.

C115 2:40 pm **An Ultra-Low Power Multi-Level Power-on Reset for Fine-Grained Power Management Strategies**

Luis E. Rueda G., Nestor Cuevas and Elkim Roa

This paper proposes a multi-level POR circuit with programmable voltage thresholds, that can operate in different fine-grained power management strategies. The POR is designed in a 0.18µm standard-logic CMOS technology, and occupies an area of 110µm x 70µm. Simulations results show a robust performance over process and temperature variations (PVT), rising times ranging from 1µs to 1s, and different supply values, while consuming a current of 19nA.

C37 3:00 pm **Output Voltage Regulation for dc-dc Buck Converters: a Passivity-Based PI Design**

Walter Gil, Oscar Montoya, Alejandro Garces, Federico Sierra and G Magaldi

This paper presents a global tracking passivity-based proportional-integral (PI) control for output voltage regulation of a dc-dc Buck converter. The proposed controller is based on passivity formulation since dc-dc Buck converter has a passive structure in open-loop. Additionally, the controller takes advantage of the PI actions to design a control law that guarantees asymptotically stability in the Lyapunov's sense under closed-loop operation. The proposed controller does not depend on the parameters, which makes it a robust controller. The robustness of the proposed controller is checked by comparing its dynamical performance in front of a conventional PID controller. All simulation results are fulfilled via MATLAB software.

C41 3:20 pm **Reliability Assessment in Transmission Considering Intermittent Energy Sources**

Alfredo Tobon

Current power systems face different types of problems nowadays, such as: the balance in adequacy of the resources, security, grid reliability, stability and the economy, to name a few. This paper deals with the problems in reliability imposed onto the grid by generation with intermittent energy resources, i.e. wind and solar energy. Power systems with high penetration grid connected power generators that use an energy source which is not available because of its random nature, can be studied from a different point of view. This paper presents the results of a study done on a reliability test power system that takes into account, first how the system behaves in terms of reliability indexes with conventional energy resources (Fossil, Nuclear and Hydropower), Then the system is presented introducing wind power and solar power. The evaluation of the system was performed by means of computational modeling and can potentially be applied to other test systems.

Session 6-4: LAEDC - Modeling

Wednesday, February 27, 2:00 pm, Pamba 3 Room

Session Chair:

E10 2:00 pm **Resistive Switching Model of OxRAM Devices Based on Intrinsic Electrical Parameters**

Silvana Guitarra, Lionel Trojman and Laurent Raymond

In this work, a model for the resistive switching of ReRAM devices that considers the electrical signal of the measurement element is developed. This model works for bipolar devices that have filamentary-type conduction and it is based on the circuit representation of the conductive filament (CF). The stochastic nature of the switching process, observed in experimental data, has been included by using a switching probability to control CF changes, and therefore, the ReRAM's resistive state. For calibration, the analysis of current-voltage curves of devices of six different areas (nm2 range) has been done. Good agreement between the experimental results and the model simulation were found.

E15 2:20 pm **Modeling Short-Channel Effects for Design by Hand with MOSFET Series Association.**
Eliyas Mehdipour, Ademir Costa, Fabian de Andrade, Maicon Pereira, Edson Santana and Ana Isabela Cunha

This work addresses the impact of short-channel effects in the series association of MOS transistors. It has been observed that the simulation results obtained through the use of series association of short transistors in submicron technologies greatly diverge from the obtained through the use of a single device with equal total length. A simple procedure is proposed to circumvent this problem in the design by hand of CMOS analog circuits applying an improved compact MOSFET model to series associations of devices. Simple current sinks and sources are dimensioned and simulated in order to assess the reliability of the design methodology with the improved model.

E19 2:40 pm **Influence of fin width and back bias on the low- frequency noise of long channel SOI nanowires**
Allan Molto, Bruna Paz and Marcelo Pavanello

This work studies the influence of fin width and back bias on the low-frequency noise of long channel fully depleted SOI nanowires. Devices with fin widths of 20nm, 45nm and 105nm were studied under different back bias (Vsub) conditions, varying Vsub from -40V to 40V. Nanowires operate in linear regime with gate voltage overdrive varying from 0mV to 200mV. Results show lowfrequency noise increase for both positive and negative back bias for long channel devices. For the input referred noise power spectral density as a function of Wfin, it was possible to observe a slight increase of SVG with Wfin decrease.

E20 3:00 pm **Verilog-A Implementation of Static and Dynamic Trigate Junctionless Nanowire Transistor Compact Model**
Cláudio V Moreira, Renan Trevisoli and Marcelo Antonio Pavanello

This paper presents the results of static and dynamic compact model of trigate junctionless nanowire transistor implementation in Verilog-A language to allow SPICE circuits simulations. The model implementation for n-type and p-type junctionless transistors has been compared with 3D Technology Computer-Aided Design (TCAD) simulations for several biases, doping concentrations, channel length and fin width, showing good agreement.

3:40 pm **Closing Ceremony**
Wednesday, February 27, Uruma Room